

# A Low Noise Amplifier Optimized for a GPS Receiver RF Front End

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## Abstract

A cascode LNA was optimized for a GPS receiver radio frequency front end using a 0.18  $\mu\text{m}$  CMOS technology. By careful choice of device geometry, gate and source degeneration inductors, a fully integrated LNA can be optimized to have a low noise figure, a high voltage gain and a wide dynamic range. The optimized LNA has a 1.512 dB noise figure, a  $-42.05$  dB  $S_{11}$ , a 20.04 dB voltage gain a  $-19.82$  dB input referred 1-dB compression point and a  $-5.49$  dBm third order input intercept point, with a 11.6 mW power consumption.

## 1. Introduction

The first stage of a radio receiver is usually a low noise amplifier (LNA). Apart from its low noise performance, which is crucial for a high performance radio frequency (RF) front end, an LNA plays an important role in impedance matching. Although the design of a high performance LNA is usually application dependant, factors such as gain, noise, power consumption, linearity and stability, determine its optimisation.

In general, for a given circuit, noise performance optimization conflicts with impedance matching. Therefore depending on applications, designers usually have to compromise noise performance due to restrictions on power consumption, input impedance matching and voltage gain of the LNAs [2].

In recent years, a lot of effort has been put into the design of LNAs to explore the lowest possible noise figure while trying to push linearity to its highest possible limit [3-7]. Most state-of-art LNAs have noise figures above 1.6 dB, but seldom do these solutions obtain voltage gains (measured as either  $S_{21}$  or available gain) larger than 16 dB. Furthermore large power consumption frequently occurs in these designs, especially when linearity is demanding. Remarkably, in recent years the noise figures of LNAs have been pushed below 1 dB [8], yet their voltage gains are usually well below 10 dB, making practical applications of these designs difficult.

According to noise theory based on a cascaded multiport network model, the noise performance for a given circuit is largely determined by the first few stages of the circuit. That is,

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_{A1}} + \dots + \frac{F_k - 1}{G_{A1}G_{A2} \dots G_{A(k-1)}} + \dots \quad (1)$$

where  $F_{tot}$  is the total noise factor of a given circuit, and  $F_k$  and  $G_{Ak}$  are the noise factor and power gain of the  $k$ -th stage of the circuit, respectively [1]. In light of this theory, the overall noise performance of a circuit is closely related to the power gains of these first few stages. The fact that an LNA is usually followed by a mixer – the noisiest stage in an RF receiver front end from a system's point of view – suggests that the gain of an LNA is, in a sense, equally as important as its noise performance. A higher power gain from an LNA can relax to some extent the restriction on the noise performance of subsequent noisy stages.

In this paper, an LNA was designed and simulated for a GPS receiver RF front end. The carrier frequency of GPS signals for civil applications is 1575.42 MHz. Typically GPS signals received at an antenna near the surface of the earth are in the order of  $-130$  dBm while the SNR is  $-19$  dB for the 2 MHz bandwidth. This extremely weak signal level puts a strong restriction on the noise performance of the front end.

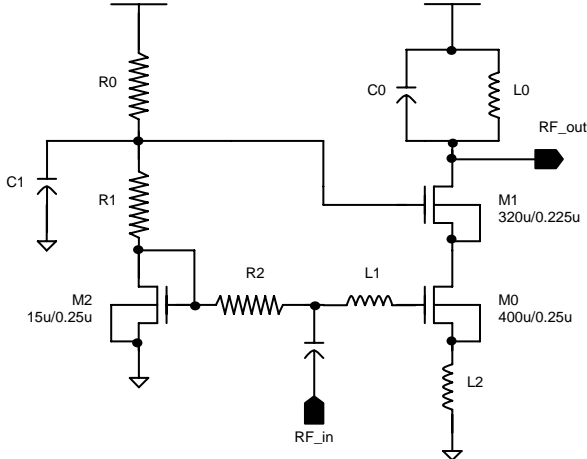
The design of our LNA focuses on the noise performance, impedance matching, high voltage gain and high linearity for a rail-to-rail supply voltage of 1.3 V.

## 2. Circuit design and considerations

A single-ended LNA was designed using a 0.18  $\mu\text{m}$  CMOS technology (TSMC CM018 process). The supply voltage was chosen to be 1.3V. The TSMC PDK for Cadence provided by the manufacturer was used as design and simulation tools. The complete schematic of the LNA is shown in Figure 1.

As the noise from the digital baseband can interfere with RF signals in an LNA via the substrate, a differential circuit topology can be used to cancel the coupling noise

in its two branches. However, to reduce power consumption a single-ended LNA was preferred for our GPS receiver RF front end. To minimize noise coupling through substrate, all three NMOS transistors were built in deep n-wells.



**Figure 1. Schematic of the LNA optimised for a GPS receiver RF front end**

According to the classical noise theory based on two-port noise network analysis, the noise factor  $F$  of a circuit can be expressed as:

$$F = F_{\min} + \frac{R_n}{G_s} \left[ (G_s - G_{opt})^2 + (B_s - B_{opt})^2 \right] \quad (2)$$

where  $F_{\min}$  is the minimum noise factor,  $G_s$  and  $B_s$  are the real and imaginary parts of the source admittance respectively,  $G_{opt}$  and  $B_{opt}$  are the real and imaginary parts of the optimum source admittance for noise, and  $R_n$  is the equivalent noise resistance [1, 2]. The minimum noise figure,  $F_{\min}$ , for a given MOS transistor is not dependant on its width,  $W$ , however according to [8],  $R_n$  is inversely proportional to  $W$ , while both  $G_{opt}$  and  $B_{opt}$  are directly proportional to  $W$ . From equation (2), we can see that for the optimum noise figure, the difference between the source admittance and the optimum source admittance needs to be minimized. As the source admittance is normally larger than the optimum source admittance, increasing the optimum source admittance by increasing  $W$  is desirable. Although  $R_n$  is inversely proportional to  $W$ , the improvement obtained from this admittance match will likely be larger. Accordingly, the widths of the two NMOS transistors, M0 and M1, were both chosen to be large. On the other hand, the width of M0 will also affect the input impedance of the LNA. In particular, increasing M0's width significantly shifts the minimum value in the  $S_{11}$  plot to lower frequencies. The

width of M1 has little impact on  $S_{11}$ . To make the current density in the two NMOS transistors comparable in this cascode configuration, while optimizing the overall performance of the LNA, the widths were chosen to be  $400 \mu\text{m}$  for the common source NMOS transistor M0 and  $320 \mu\text{m}$  for the cascode NMOS transistor M1. To reduce power consumption while aiming for a noise figure around 1.5 dB, the lengths of M0 and M1 were chosen to be  $0.25 \mu\text{m}$  and  $0.225 \mu\text{m}$ , respectively.

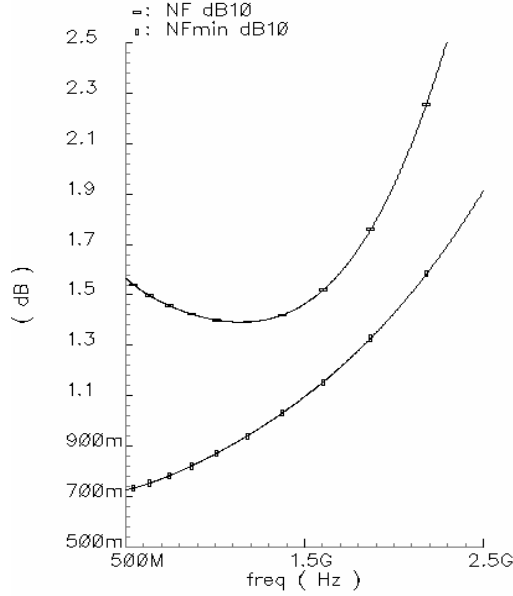
Three parasitic capacitances,  $C_{sb}$ ,  $C_{db}$ , and  $C_{gs}$ , affect the input impedance significantly. Splitting the large transistor into  $n$  parallel segments (fingers), may increase  $C_{gs}$  slightly but, helps to reduce  $C_{sb}$  and  $C_{db}$  by a factor of  $(n+2)/2n$  if  $n$  is even, or  $(n+1)/2n$  if  $n$  is odd. For a MOS transistor of given width,  $C_{sb}$  and  $C_{db}$  can be reduced by  $\sim 50\%$  when the number of fingers is large. To improve the minimum value in the  $S_{11}$  plot, which is an important indicator of input impedance matching, M0 and M1 are segmented uniformly into 50 and 40 fingers, respectively.

By connecting the bulk of each of the MOS transistors, M0 and M1, to its source, rather than to ground,  $C_{sb}$  can be by-passed and hence its effect on input impedance seen by RF signals from the source of the transistor is reduced. Simulations showed that, without any changes in the geometries of the components in this circuit, source-bulk connections improved the  $S_{11}$  value. Moreover, the noise figure was also slightly improved.

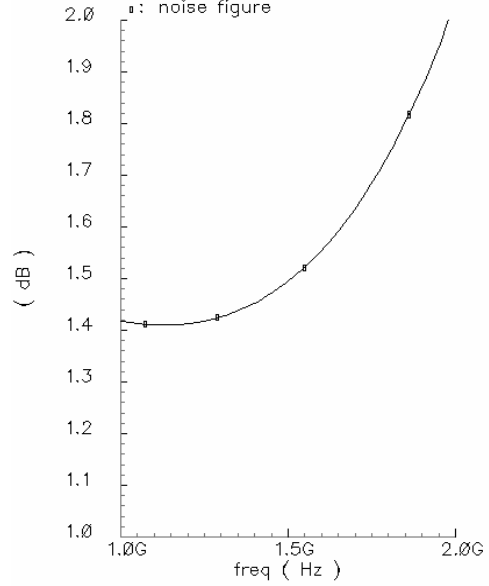
The DC biasing network for the common source MOS transistor M0 was optimized as follows. The NMOS transistor M2 was built in a deep n-well, with its width and length being  $15 \mu\text{m}$  and  $250 \text{ nm}$ , respectively. The gate was divided into 2 fingers. Resistors R0, R1 and R2 were chosen to be  $524 \Omega$ ,  $1.156 \text{ K}\Omega$  and  $3.058 \text{ K}\Omega$ , respectively. The diode connected NMOS transistor M2, R0 and R1 produced a  $0.65 \text{ V}$  DC biasing voltage at the gate of the common source NMOS transistor M0.

The best noise figure and voltage gain  $S_{21}$  of the LNA were obtained when the gate of M1 was biased directly from the power supply, which was  $1.3 \text{ V}$ , for the current design. However, to optimize the linearity of the LNA, the biasing voltage was chosen to be  $1.1 \text{ V}$ , which was produced by the voltage divider R0 and R1 in the circuit. The penalties for this biasing voltage were that noise figure increased by  $0.009 \text{ dB}$  while  $S_{21}$  decreased by  $0.16 \text{ dB}$ . Moreover, the large real impedance seen by the gate of the cascode NMOS transistor M1, due to the resistive divider used in the biasing network, destroyed the impedance matching obtained when M1 was biased directly from the voltage supply.

The equivalent impedance of the DC biasing network can be modeled by a resistor  $R_B$  connected in parallel with a capacitor  $C_B$ . The impedance  $Z_B$  seen by the gate



(a) Noise figure and minimum noise figure in small signal analysis



(b) Noise figure in large signal analysis

Figure 2. Noise figure and minimum noise figure

of M1 is simply

$$Z_B = \frac{1}{j\omega C_B + \frac{1}{R_B}} \quad (3)$$

To make  $Z_B$  as close as possible to zero,  $j\omega C_B$  has to dominate the denominator and, in particular,  $\omega C_B$  has to be much greater than unity. Accordingly, a large capacitor can be used in the resistive voltage divider to provide a low impedance path to RF signals leaked into the biasing network through  $C_{gs}$  of M1. The low impedance seen by M1's gate at RF frequencies helps to stabilize the biasing voltage of the gate and hence maintain the original shape of the  $S_{11}$  curve. Simulations showed that a good  $S_{11}$  curve with a deep valley centered about 1.575 GHz was restored when the capacitance of C1 was larger than 30 pF. A 40.9 pF was used in this design.

As a result of reducing the DC biasing voltage of M1 by 200 mV, the current flowing through the two NMOS transistors in cascode configuration was reduced, due to the finite drain resistance of M0, and accordingly the power consumption of the LNA decreased by 4.1%.

Without any load capacitance and parasitic capacitance, the frequency  $f_0$  of the resonance tank in the LNA can be estimated using the following relation

$$f_0 = \frac{1}{2\pi\sqrt{L_0 C_0}} \quad (4)$$

To produce high output impedance for GPS signals so that the LNA can obtain a high voltage gain, the capacitor C0 was chosen to be 827 fF and the inductor L0 5.7 nH.

Together with the load capacitance and parasitic capacitances of the transistors, they provided a resonance frequency about 1.575 GHz, which was very stable even with large variations in the geometries of the two MOS transistors and other components in the design.

Two inductors, L1 and L2, were used for input impedance matching. The choices for these two inductors significantly influences the noise figure. Moreover, the inductance of L1 is closely related to the value of  $S_{11}$ . In particular, as the inductance of L1 is increased, the  $S_{11}$  minimum shifts significantly towards the lower frequency end of the spectrum while the noise figure of the circuit increases sharply. For our purpose L1 was chosen to have an inductance of 10.64 nH.

On the other hand, the source degeneration inductor L2 affects the input impedance and noise figure in a manner quite different from that of L1. Increasing L2's inductance raises the noise figure in general.  $S_{11}$  approached its minimum value when L2's inductance was around 627 pH while the  $S_{11}$  curve hardly shifted in response to the variations in L2's inductance. For our GPS receiver, the inductance of L2 was chosen to be 627.5 pH.

### 3. Simulation results

Unless otherwise stated, in the following simulations -130 dBm was used as the input power to the LNA, which is a typical GPS signal power level received by a ground based station.

As shown in Figure 2 (a) and (b), the noise figure of

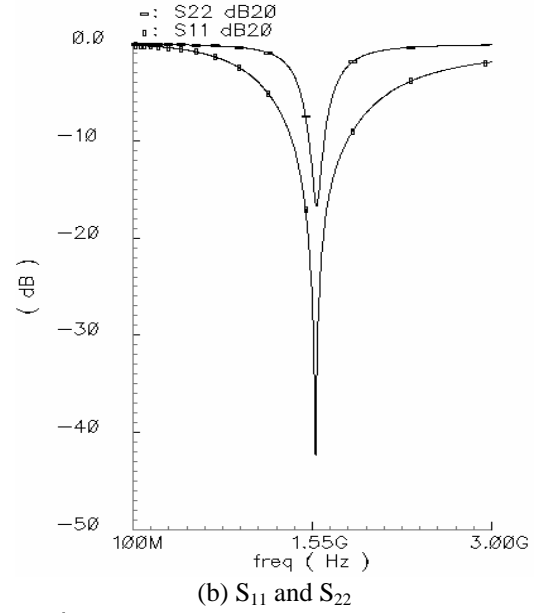
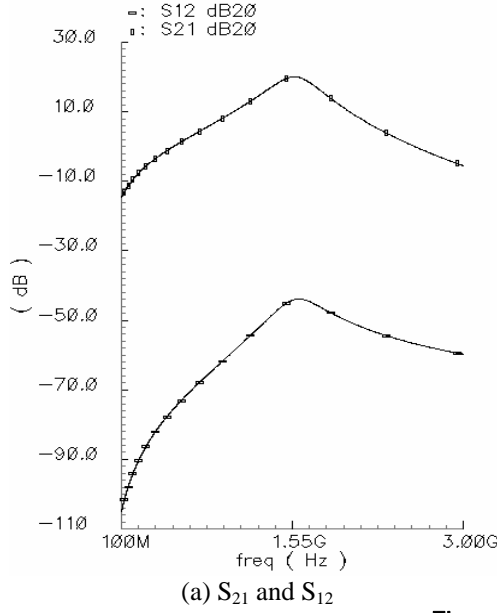


Figure 3. Scattering parameters

the LNA at 1.575 GHz was 1.502 dB and 1.524 dB in small signal analysis and large signal analysis, respectively. Simulation also showed that when the supply voltage was increased toward 1.8 V, the noise figure could be pushed down toward an even lower level around 1.3 dB.

The voltage gain of the LNA, shown in Figure 3(a) as  $S_{21}$ , was 20.04 dB at 1.575 GHz.

Furthermore,  $S_{12}$ , which was shown as -43.99 dB at 1.575 GHz, guarantees unilateral behaviour of the LNA, or in other words, the signal leakage from its output port back into its input port is negligible and will not interfere with the input signals from the antenna of the receiver.

As an indicator of impedance match,  $S_{11}$ , shown in Figure 3(b), was -42.05 dB at 1.575 GHz, which implied that the power reflected by the LNA was well below 0.8% of the input GPS signal power.

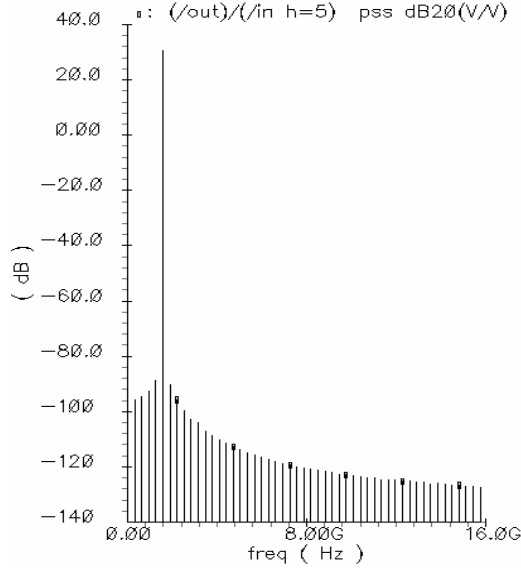
Simulations also showed that  $S_{22}$ , which is an indicator of the reflection of signals at the output port of the LNA, was -16.38 dB.

When the input power was -130 dBm, the periodic steady state response shown in Figure 4(a) indicated that a GPS signal received a 30.53 dB voltage gain while all sideband signals had voltage gains well below -80 dB. To examine the steady state response of the LNA with large input signal power, a -30 dBm signal was used in the simulation shown in Figure 4(b). The analysis showed in this case that the voltage gain of the LNA was 30.51 dB and all major sidebands had voltage gains lower than -22.81 dB, which made the output GPS signals at least 53 dB stronger than all sideband signals.

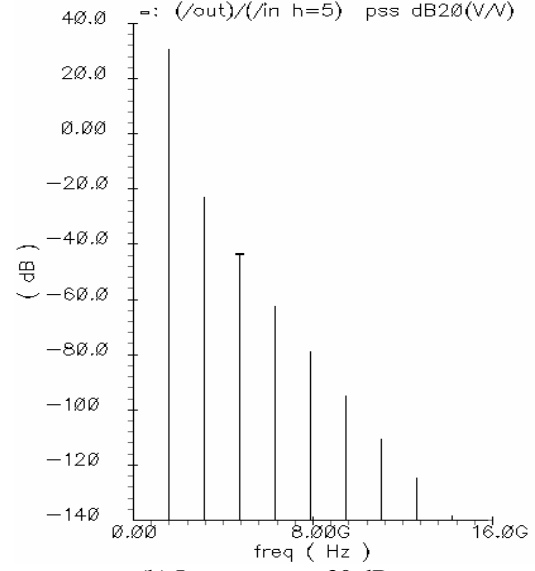
The input referred 1-dB compression point, as shown in Figure 5, was -19.82 dBm. The IIP3 point, when extrapolated from a relatively large input signal level of -60 dBm, was -5.49 dBm (Figure 6). In summary, these results indicate a relatively wide dynamic range for the LNA, which is essential for a GPS receiver operating in a noisy environment.

In the current design, the power consumption of the LNA, including that of its biasing components, was 11.6 mW. Simulations showed that the power consumption of the LNA could be reduced by 10-20% by increasing the length of cascade NMOS transistor. This slightly compromises the noise performance, but the noise figure of the LNA would still be well below 1.7 dB.

To test the tolerance of the LNA circuit to fabrication errors, the LNA was tested with  $\pm 5$  nm (for MOS transistors and inductors) and  $\pm 10$  nm (for capacitors) deviations from the dimensions specified in our final design. They are the smallest allowable increments for TSMC CM018 PDK. Simulations showed that in a majority of cases the performance errors introduced by these deviations remained well within  $\pm 0.003$  dB,  $\pm 0.031$  dB,  $\pm 0.089$  dB,  $\pm 0.032$  dB,  $\pm 0.025$  dB of the designed values for  $F$ ,  $S_{21}$ ,  $S_{11}$ ,  $S_{22}$  and  $S_{12}$ , respectively. The worst deviation occurred when the length of the common source MOS transistor M0 deviated from its designed value by -5 nm, where the errors were -0.005 dB, -0.13 dB and +10.83 dB in  $F$ ,  $S_{21}$  and  $S_{11}$ , respectively, while the errors in the other two scattering parameters were less than 0.05 dB.  $S_{11}$  in this case was -34.83 dB, which is still well below -30 dB. However,



(a) Input power -130 dBm



(b) Input power -30 dBm

Figure 4. Periodic steady state analysis of voltage gain

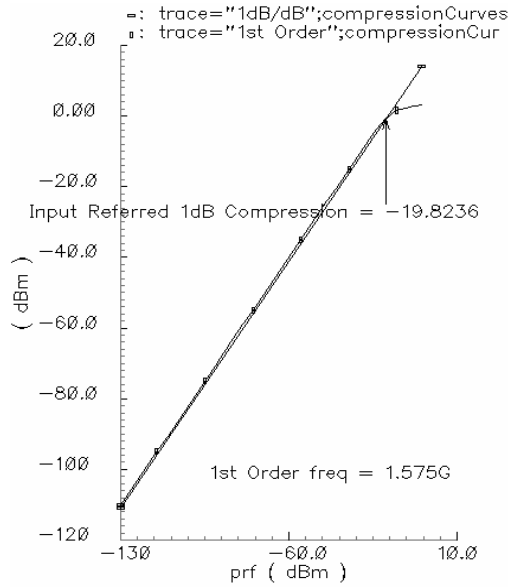


Figure 5. Input referred 1-dB Compression Point

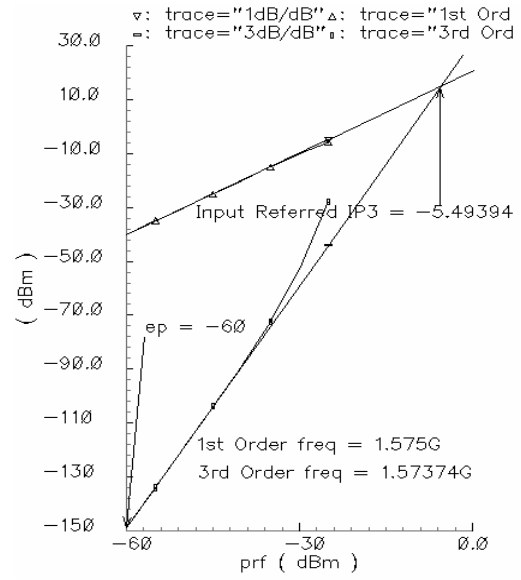


Figure 6. Third-Order Input Intercept Point

due to M0's large width and segmentation, it is expected that fabrication errors in its length will largely average out. Hence we believe that the performance of the LNA circuit is reasonably well predicted by the simulation results. The cascode MOS transistor M1 showed a much better tolerance to the errors in its length, a  $\pm 5$  nm error made  $S_{11}$  and  $S_{22}$  vary less than +0.29 dB and -0.02 dB, respectively, and only minimally affected the noise figure,  $S_{21}$  and  $S_{12}$ .

Simulations also showed that The LNA was

unconditionally stable over a range from 100 MHz to 10 GHz.

The simulation results for the optimized LNA are summarized in table 1.

#### 4. Conclusion

A high performance narrow band LNA was designed for a GPS receiver RF front end using a 0.18  $\mu$ m CMOS technology (TSMC CM018 process) in this paper. By

controlling the gate and source degeneration inductances and the widths of the NMOS transistors, the LNA was optimized to have a 20.04 dB voltage gain, a 1.502 dB noise figure, a  $-42.04$  dB  $S_{11}$ , a  $-19.82$  dBm input referred 1-dB compression point and a  $-5.49$  dBm third-order input intercept point. Further optimization for lower power consumption can be expected by increasing the lengths of the NMOS transistors in this design and/or reducing the power consumption of the biasing circuit. Impedance matching can be improved by careful selection for transistors sizes, the inductances of the gate and source degeneration inductors.

**Table 1 Simulation results of a 1.575GHz LNA**

Parameters	Simulated Value
Frequency	1.575 GHz
Supply Voltage	1.3 V
Power Consumption	11.6 mW
Noise Figure	1.502 dB
$S_{21}$	20.04 dB
$S_{11}$	$-42.05$ dB
$S_{22}$	$-16.38$ dB
$S_{12}$	$-43.99$ dB
IIP3	$-19.82$ dBm
Input Referred 1-dB Compression	$-5.49$ dBm

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